FIG. 1

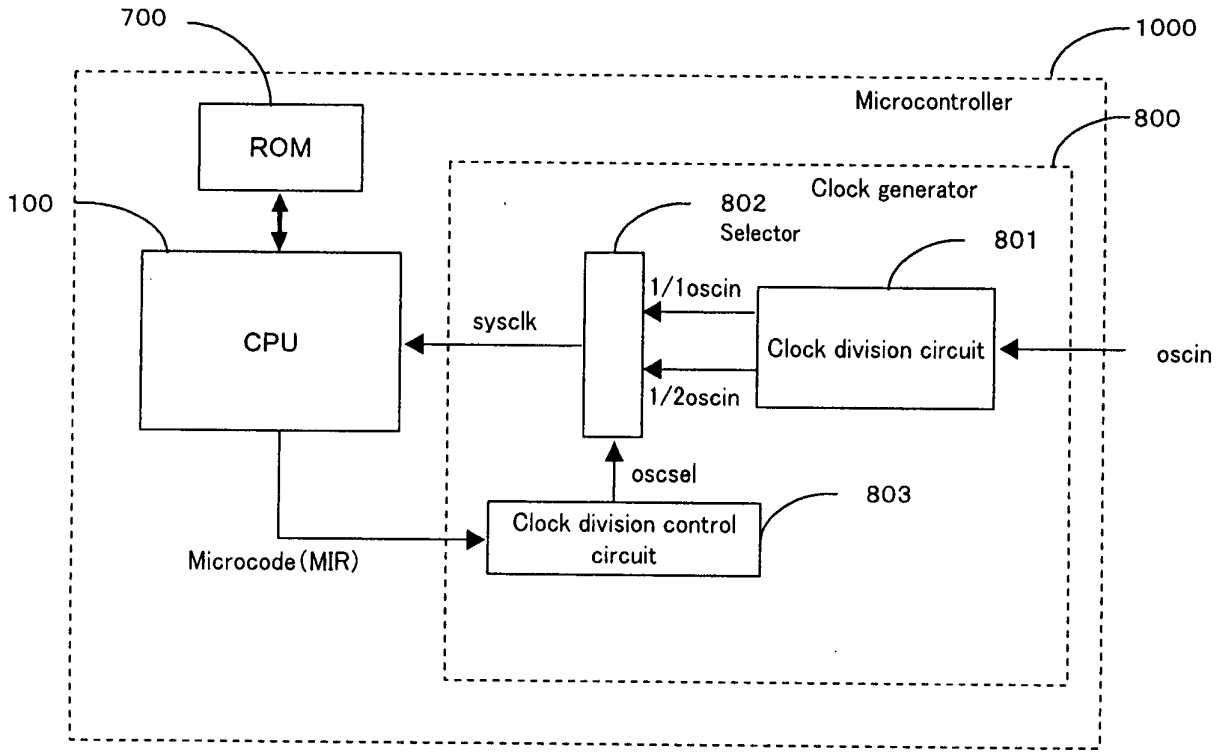

700
1000
Microcontroller
ROM
800
Clock generator
100
802
Selector
801
1/1oscin
CPU
sysclk
Clock division circuit
oscin
1/2oscin
oscsel
803
Clock division control circuit
Microcode (MIR)

FIG. 2

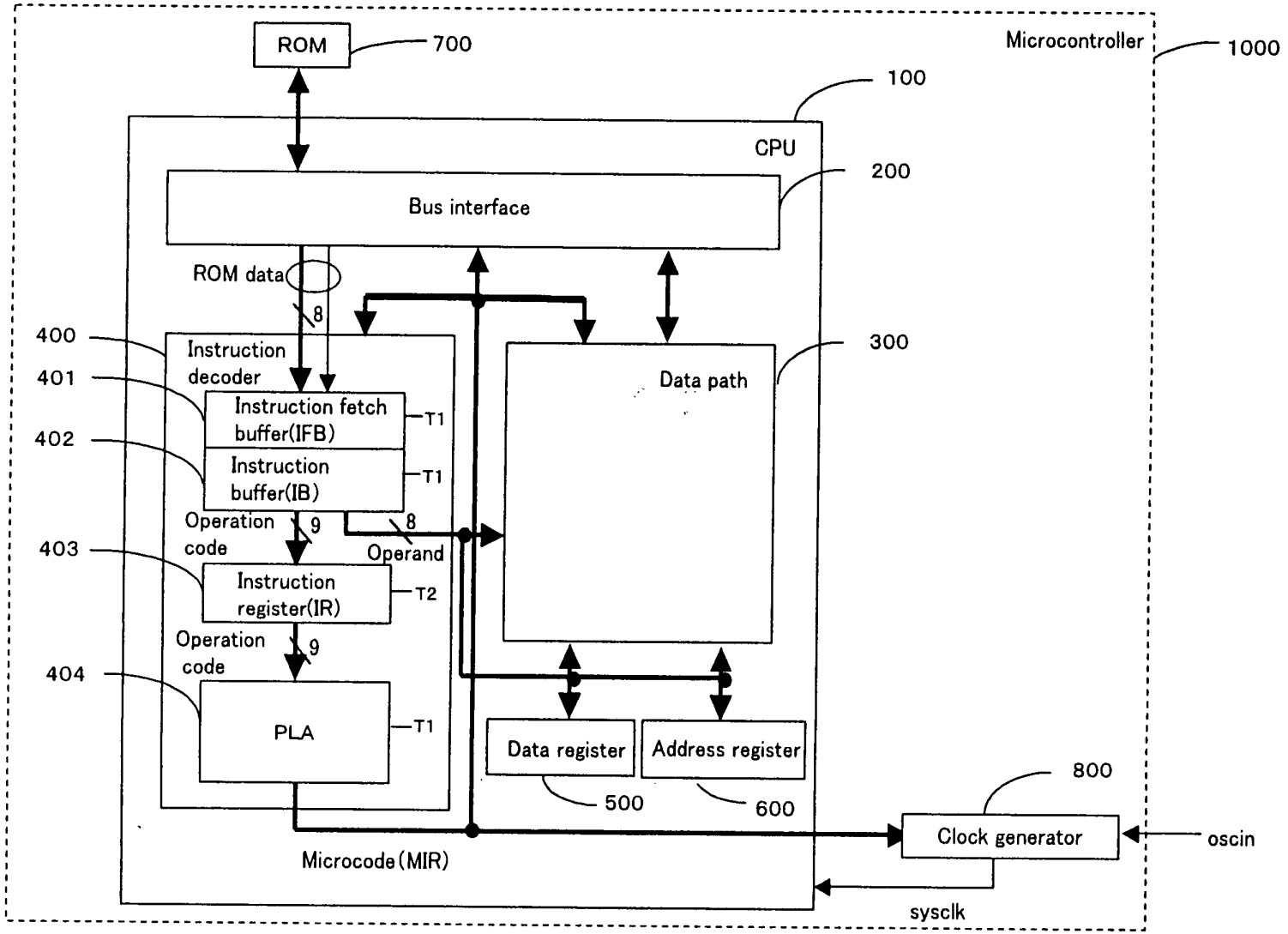

ROM
700
Microcontroller
1000
100
CPU
200
Bus interface
ROM data
8
400
Instruction decoder
401
Instruction fetch buffer(IFB)
T1
402
Instruction buffer(IB)
T1
Operation code
9
8
Operand
403
Instruction register(IR)
T2
Operation code
9
404
PLA
T1
300
Data path
Data register
Address register
500
600
800
Clock generator
oscin
Microcode(MIR)
sysclk

FIG. 3A

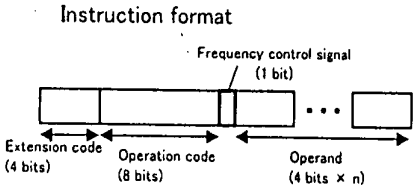


FIG. 3B

Instruction	Machine code (in nibbles) 1 2 3 4 5			
①ADD D0,D1	(0011)0111 0001*0	3-nibble 2-cycle instruction	*D0,D1:Data register	(0011)Extension code
③SUB imm8,D1	(0010)1010 0101*1 <#8....>	5-nibble 2-cycle instruction		(0010)Extension code
④SUB D0,D3	(0010)1010 0011*1	3-nibble 2-cycle instruction	*D3:Data register	(0010)Extension code
⑥ADD D2,D3	(0011)0011 0001*0	3-nibble 1-cycle instruction	*D2:Data register	(0011)Extension code
⑦AND D2,D3	(0011)0111 1011*0	3-nibble 2-cycle instruction		(0011)Extension code

Set sysclk to oscillation clock cycle of oscin

Set sysclk to oscillation clock cycle divided by two of oscin

*0: Frequency control signal for setting sysclk to oscillation clock cycle of oscin
*1: Frequency control signal for setting sysclk to oscillation clock cycle divided by two of oscin

FIG. 3C

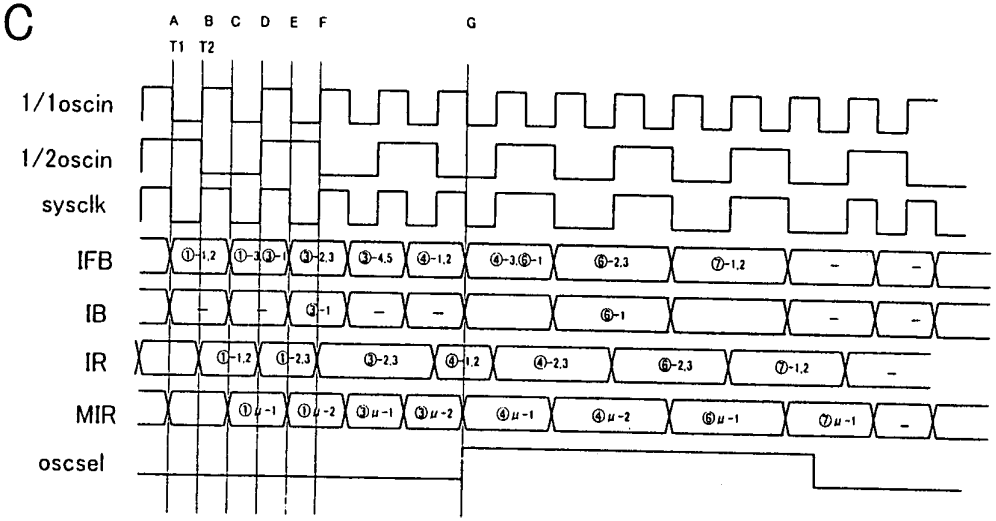


FIG. 4

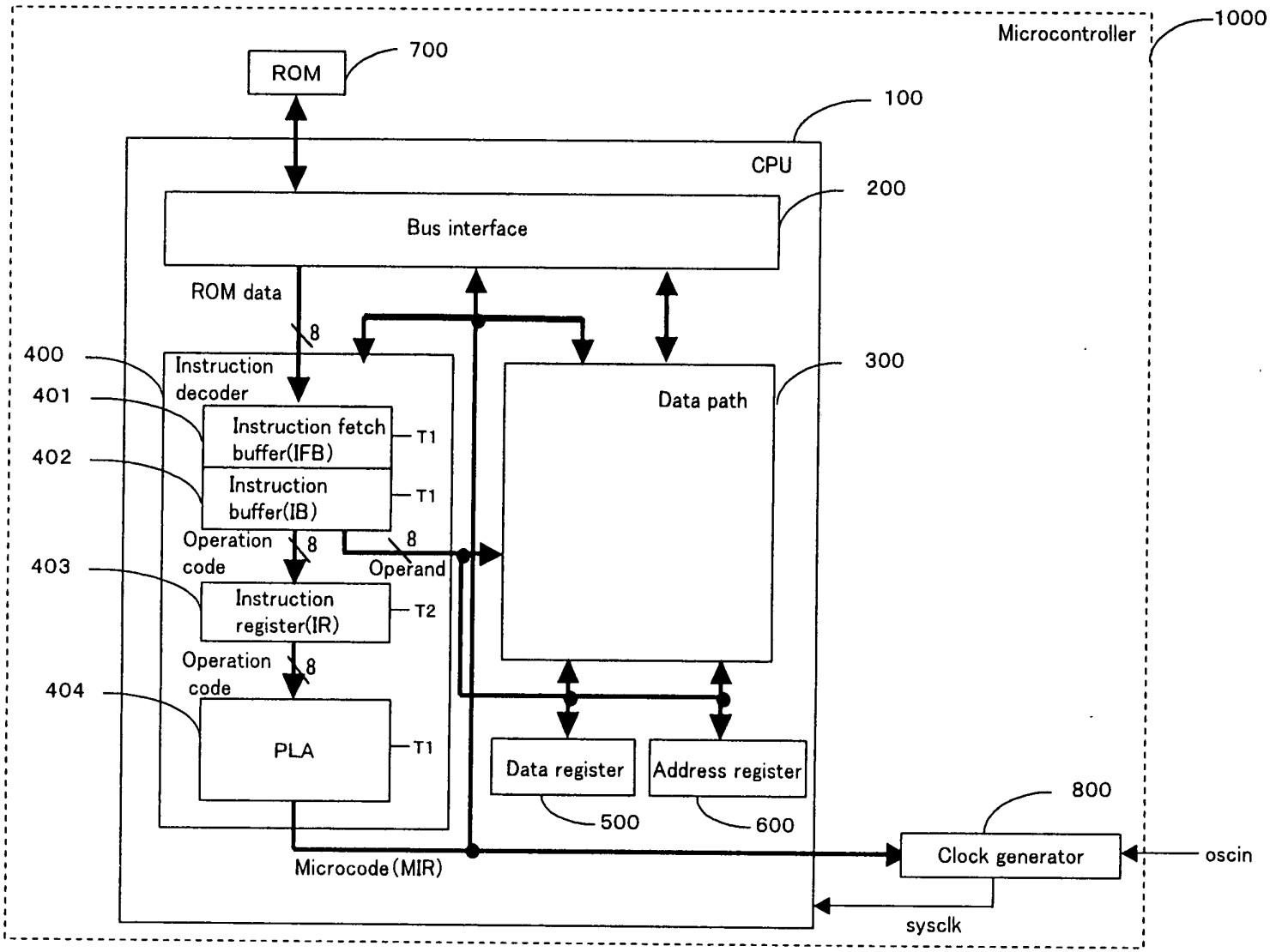
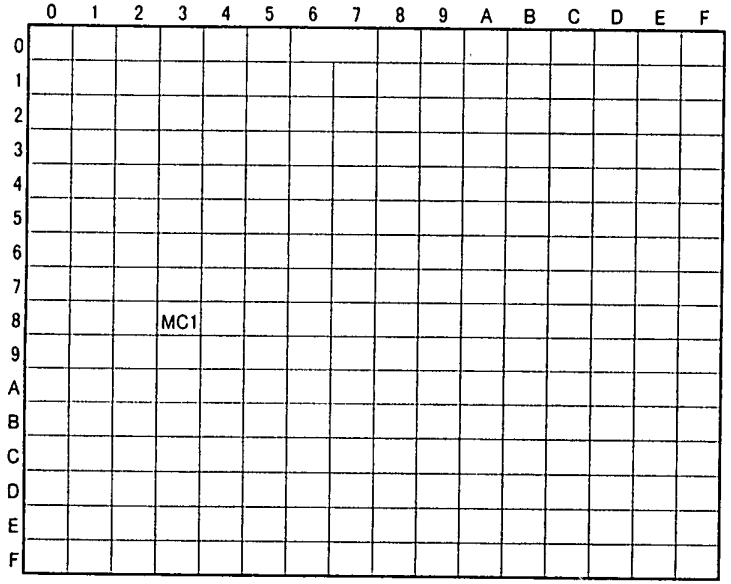

Microcontroller
1000
ROM
700
100
CPU
200
Bus interface
ROM data
8
400
Instruction decoder
401
Instruction fetch buffer(IFB)
T1
402
Instruction buffer(IB)
T1
Operation code
8
8
Operand
300
Data path
403
Instruction register(IR)
T2
Operation code
8
404
PLA
T1
Data register
500
Address register
600
800
Clock generator
oscin
sysclk
Microcode(MIR)

FIG. 5A

Instruction map A (corresponding to oscillation clock cycle)



MC1: 0011 1000 0011 ·····

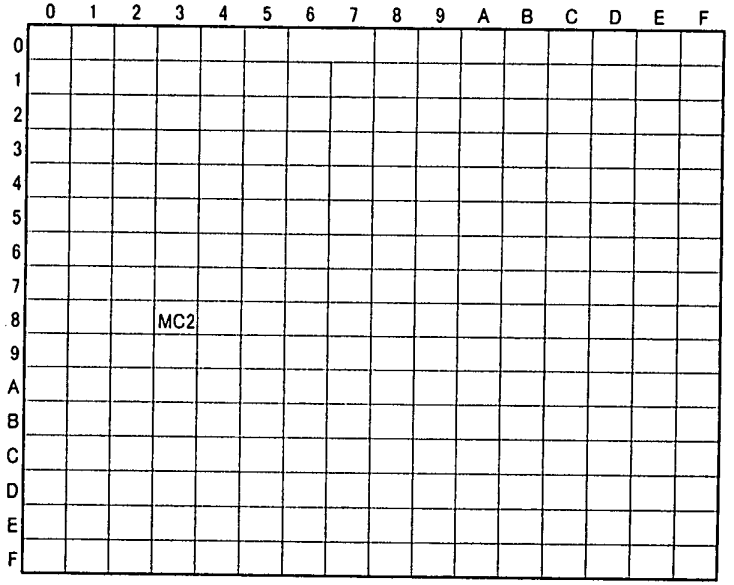
Extension code for oscillation clock cycle

Operation code

Operand

FIG. 5B

Instruction map B (corresponding to oscillation clock cycle divided by two)



MC2: 0101 1000 0011 ·····

Extension code for oscillation clock cycle divided by two

Operation code

Operand

FIG. 6A

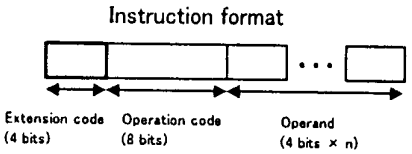


FIG. 6B

Machine code (in nibbles)

Instruction	1	2	3	4	5			
①ADD D0,D1	(0011)0011 0001					3-nibble 2-cycle instruction	*D0,D1:Data register	(0011) Extension code for oscillation clock cycle
③SUB imm8,D1	(0101)1010 0101	<#8....>				5-nibble 2-cycle instruction		(0101) Extension code for oscillation clock cycle divided by two
④SUB D0,D3	(0101)1010 0011					3-nibble 2-cycle instruction	*D3:Data register	(0101) Extension code for oscillation clock cycle divided by two
⑥ADD D2,D3	(0011)0011 0001					3-nibble 1-cycle instruction	*D2:Data register	(0011) Extension code for oscillation clock cycle
⑦AND D2,D3	(0011)0111 1011					3-nibble 2-cycle instruction		(0011) Extension code for oscillation clock cycle

Set sysclk to oscillation clock cycle of oscin

Set sysclk to oscillation clock cycle divided by two of oscin

FIG. 6C

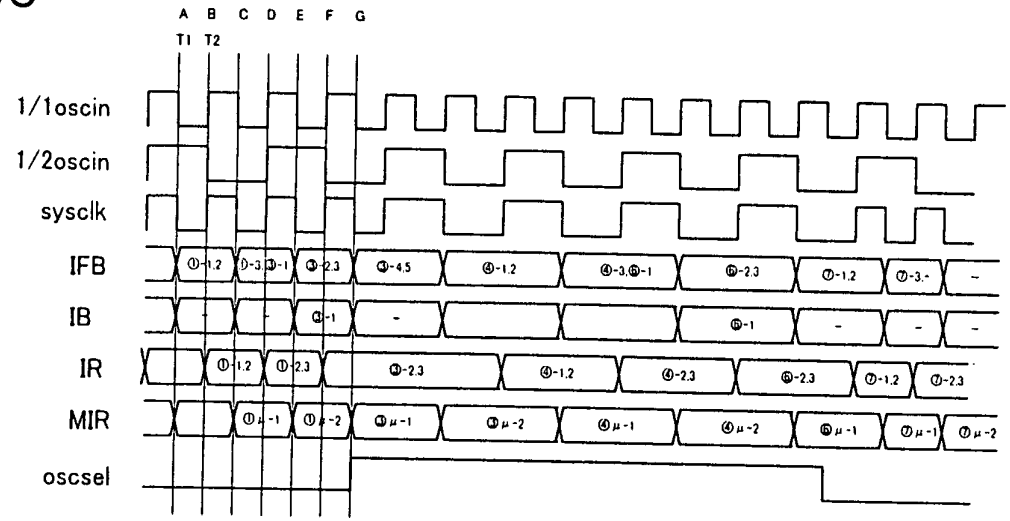


FIG. 7A

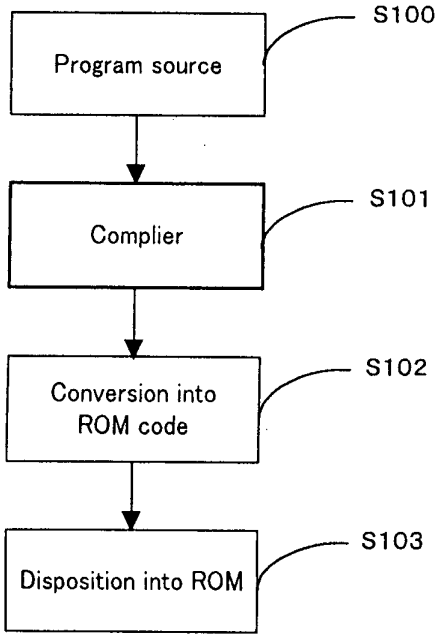


FIG. 7B

```
set fast
  ①ADD D0,D1                (0011)0111 0001*0
set slow
  ③SUB imm8,D1              (0010)1010 0101*1 <#8....>
  ④SUB D0,D3                (0010)1010 0011*1
set fast
  ⑥ADD D2,D3                (0011)0011 0001*0
  ⑦AND D2,D3                (0011)0111 1011*0
```

*0: Frequency control signal for setting sysclk to oscillation clock cycle of oscin
*1: Frequency control signal for setting sysclk to oscillation clock cycle divided by two of oscin

FIG. 8A

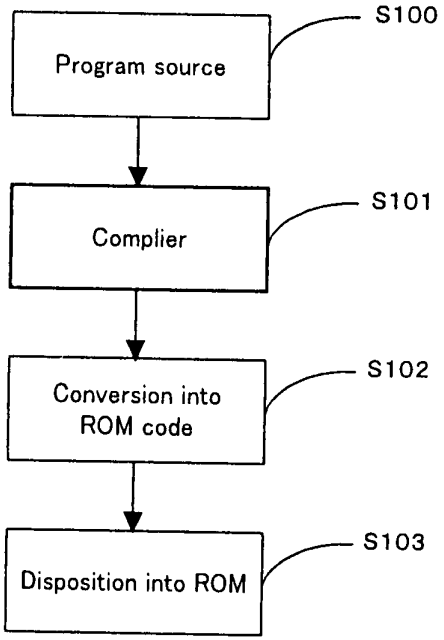


FIG. 8B

set fast/set slow + preceding not-more-than-2-cycle instruction
= add control bit to instruction code preceding set fast/set slow
set fast/set slow + preceding not-less-than-3-cycle instruction
= add control bit to instruction code succeeding set fast/set

set fast		
①ADD D0,D1	2cycles	(0011)0111 0001*1
set slow		
③SUB imm8,D1	2cycles	(0010)1010 0101*1 <#8....>
④SUB D0,D3	2cycles	(0010)1010 0011*0
set fast		
⑥ADD D2,D3	1cycle	(0011)0011 0001*0
⑦AND D2,D3	2cycles	(0011)0111 1011*0

*0: Frequency control signal for setting sysclk to oscillation clock cycle of oscin
*1: Frequency control signal for setting sysclk to oscillation clock cycle divided by two of oscin

FIG. 8C

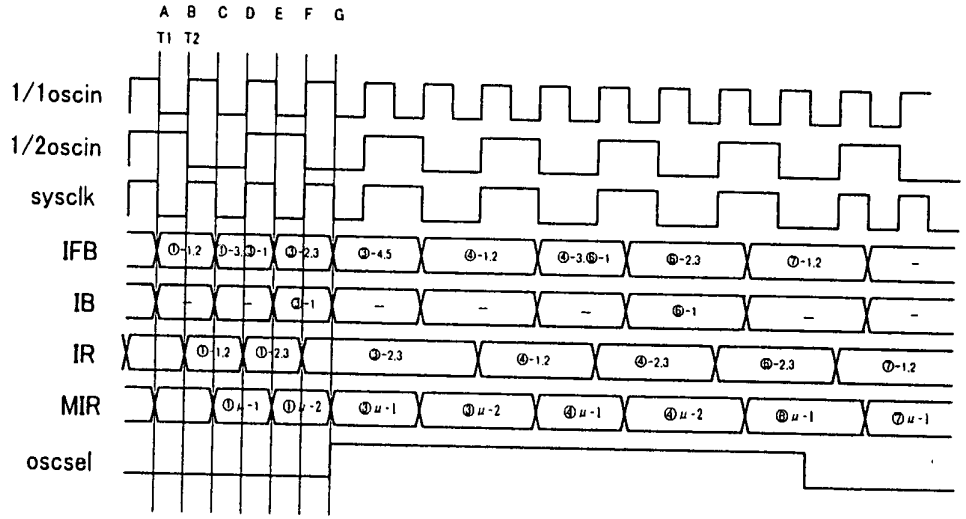


FIG. 9A

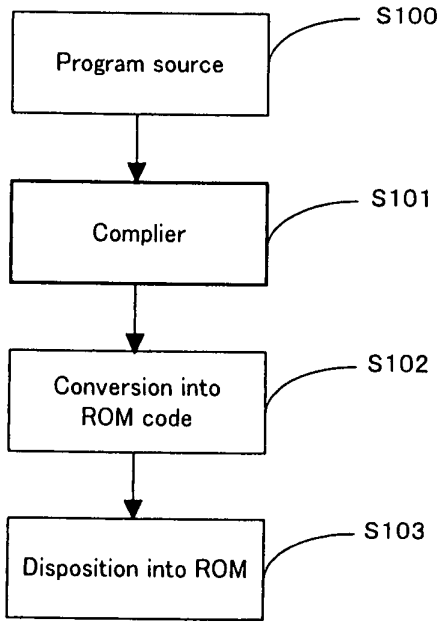


FIG. 9B

Extension codes for oscillation clock cycle: no extension code,0010,0011
Extension codes for oscillation clock cycle divided by two:0100,0101,0110

set fast + instruction = extension code for oscillation clock cycle + machine code
set slow + instruction = extension code for oscillation clock cycle divided by two + machine code

set fast	
①ADD D0,D1	(0011)0011 0001
set slow	
③SUB imm8,D1	(0101)1010 0101 <#8....>
④SUB D0,D3	(0101)1010 0011
set fast	
⑥ADD D2,D3	(0011)0011 0001
⑦AND D2,D3	(0011)0111 1011

(0011):Extension code for oscillation clock cycle
(0101): Extension code for oscillation clock cycle divided by two

FIG. 10

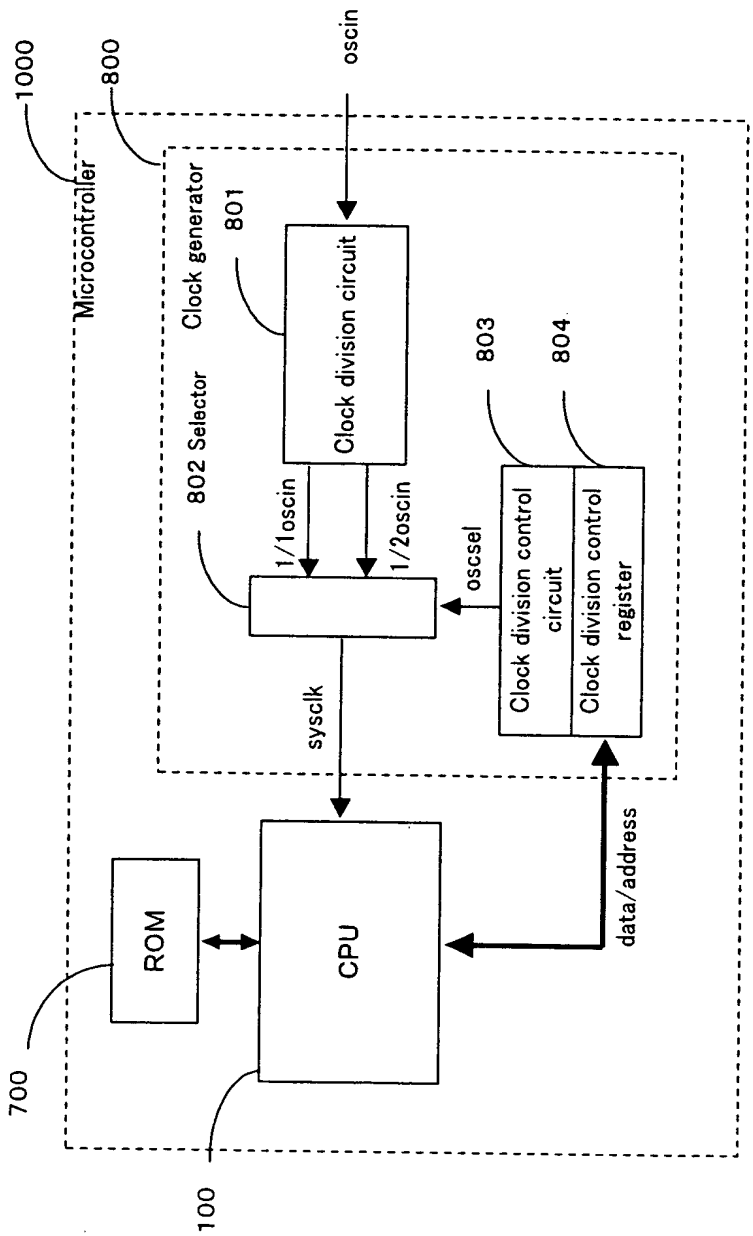

1000
Microcontroller
800
Clock generator
oscin
801
Clock division circuit
802 Selector
1/1oscin
1/2oscin
803
804
oscsel
Clock division control circuit
Clock division control register
sysclk
data/address
ROM
CPU
700
100

FIG. 11

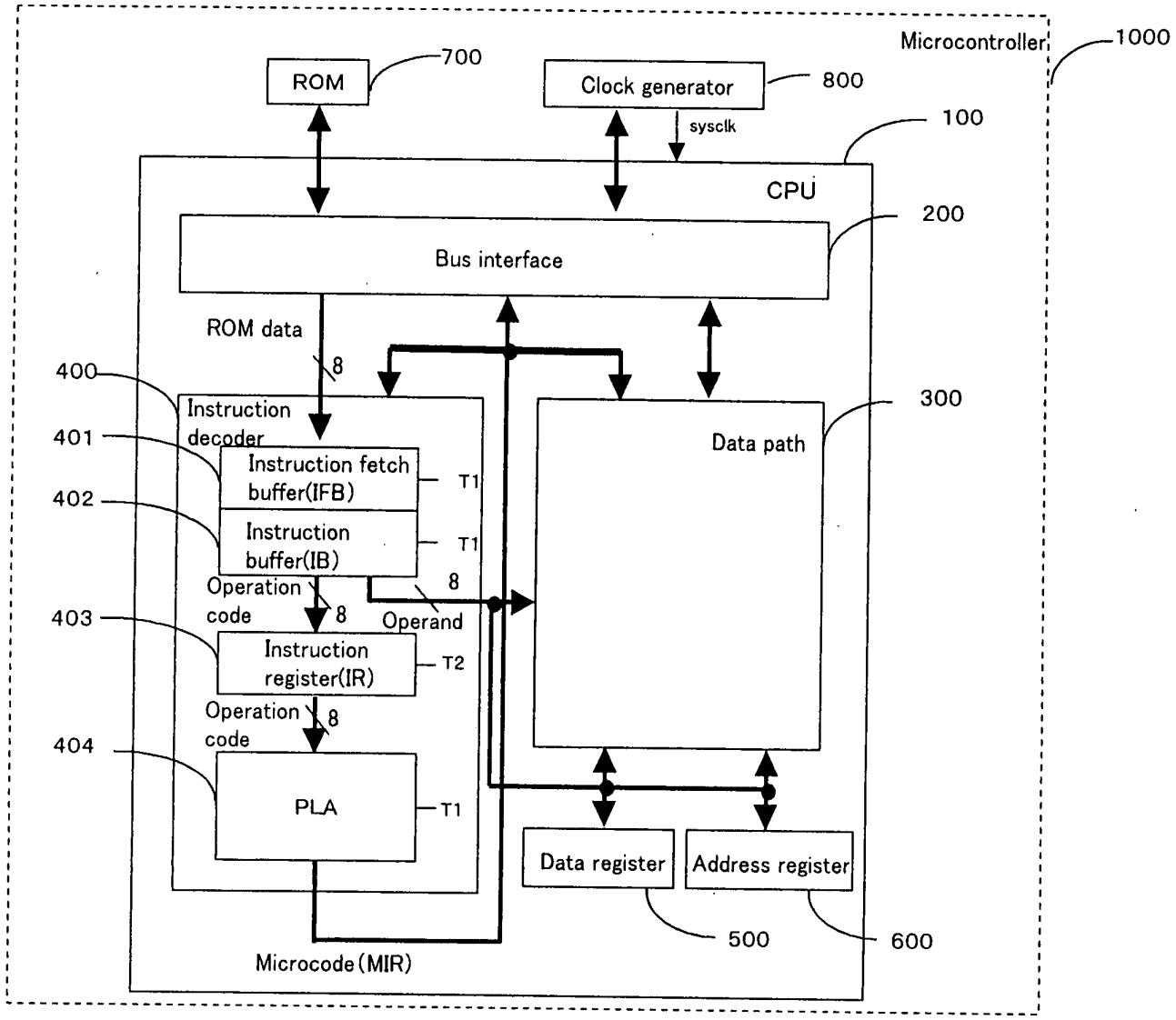

Microcontroller
1000
ROM
700
Clock generator
800
sysclk
100
CPU
200
Bus interface
ROM data
8
400
Instruction decoder
401
Instruction fetch buffer(IFB)
T1
402
Instruction buffer(IB)
T1
8
Operation code
8
Operand
403
Instruction register(IR)
T2
Operation code
8
404
PLA
T1
300
Data path
Data register
Address register
500
600
Microcode(MIR)

FIG. 12A

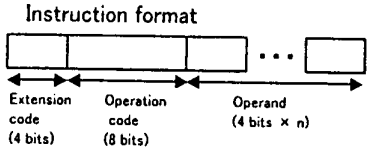


FIG. 12B

Instruction	Machine code (in nibbles) 1 2 3 4 5 6		
①ADD D0,D1	(0011)0011 0001	3-nibble 2-cycle instruction	*D0,D1:Data register *(0011) Extension code
②MOV imm8,(io8)	0000 0010 <io8 . . . ><#8 . . . .>	6-nibble 3-cycle instruction	*io8:Clock division control register ··· Change division ratio of oscin from oscillation clock cycle to oscillation clock cycle divided by two
③SUB imm8,D1	(0010)1010 0101 <#8 . . . . >	5-nibble 2-cycle instruction	*(0010)Extension code
④SUB D0,D3	(0010)1010 0011	3-nibble 2-cycle instruction	*(0010)Extension code
⑤MOV imm8,(io8)	0000 0010 <io8 . . . ><#8 . . . .>	6-nibble 3-cycle instruction	*io8:Clock division control register ··· Change division ratio of oscin from oscillation clock cycle divided by two to oscillation clock cycle
⑥ADD D2,D3	(0011)0011 0001	3-nibble 1-cycle instruction	*D2,D3:Data register *(0011) Extension code
⑦AND D2,D3	(0011)0111 1011	3-nibble 2-cycle instruction	*(0011) Extension code

Set sysclk to oscillation clock cycle of oscin

Set sysclk to oscillation clock cycle divided by two of oscin

FIG. 12C